

**AMENDMENTS**

**IN THE CLAIMS:**

*Please amend claims 1, 3-5, 21 and 22 as follows below.*

1. (Currently amended) An integrated circuit, comprising:  
~~an array of ferroelectric memory cells, each cell having a capacitor stack having an upper electrode, a lower electrode, a lower conductive barrier layer underlying the lower electrode, and a single ferroelectric core layer with disposed between the upper and lower electrodes, wherein the single ferroelectric core layer comprises a crystallization in the (001) family, wherein at least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack, the integrated circuit further comprising wherein at least one of the capacitor stacks comprises a conductive contact formed thereunder and at least one of the capacitor stacks, wherein the conductive contact has a cross section near at a contact portion with of the that contacts a bottom portion of the capacitor stack that is about as large or larger than that of the ferroelectric core[[s]] layer.~~
2. (Original) The integrated circuit of claim 1, wherein from about 45 to about 75% of the domains are functionally oriented with respect to the capacitor stack.
3. (Currently amended) The integrated circuit of claim 1, wherein the ferroelectric core[[s]] layer comprises ~~a~~ are PZT cores and the PZT of each core has ~~having~~ a switched polarization of at least about 60  $\mu\text{C}/\text{cm}^2$ .
4. (Currently amended) The integrated circuit of claim 1, further comprising:  
a dielectric layer covering the array of memory cells, the dielectric layer having a conductive contact over each ferroelectric core, the conductive contacts each having a cross section about as large or larger than that of the ferroelectric core[[s]] layer.

5. (Currently amended) The integrated circuit of claim 1, wherein electrodes adjacent opposing sides of the ferroelectric core[[s]] layer have a collective thickness of at least about 200 nm thick.

6-20. (cancelled)

21. (Currently amended) The integrated circuit of claim 1, further comprising: a dielectric layer covering the array of memory cells, the dielectric layer having an additional conductive contact over each ferroelectric core layer and upper electrode, the additional conductive contacts each having a cross section about as large or larger than that of the ferroelectric core[[s]] layer and extending through said dielectric layer to a metal interconnect layer.

22. (Currently amended) An integrated circuit, comprising:  
an array of ferroelectric memory cells, each cell having a capacitor stack comprising:  
a lower conductive barrier layer;  
a lower electrode over the lower conductive barrier layer;  
a single ferroelectric core layer with disposed between the upper and lower electrodes, wherein the single ferroelectric core layer comprises crystallization in the (001) family, wherein at least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack;  
an upper electrode over the single ferroelectric core layer; and  
an upper barrier over the upper electrode;  
wherein at least one of the capacitor stackthe integrated circuit further comprises a first conductive contact formed over the capacitor stack, and a second conductive contact formed under the capacitor stack, and wherein the first and second conductive contacts each have a cross section near at a contact portion of the capacitor stack that is about as large or larger than that of the ferroelectric core[[s]] layer.